

**AMENDMENTS TO THE CLAIMS**

This listing of claims replaces all prior versions, and listing, of claims in the specification:

1. (Currently amended) A circuit coupled to an output device, the circuit comprising at least one transistor device comprising at least one p-channel device, said at least one transistor device adapted to limit a duration of a high voltage across the output device thereby reducing hot carrier injection stress across the output device.

2. (Original) The circuit of Claim 1, further comprising two stacked transistor devices coupled to the output device.

3. (Currently Amended) The circuit of Claim 1, wherein said at least one p-channel device is ~~transistors~~ coupled to the output device.

4. (Currently Amended) The circuit of Claim ~~2~~ 4, wherein said two stacked transistor ~~device comprises~~ devices comprise two stacked p-channel ~~transistors~~ devices coupled to the output device.

5. (Original) The circuit of Claim 1, wherein the output device comprises at least one n-channel output transistor.

6. (Currently Amended) The circuit of Claim 1, wherein the output device comprises two stacked n-channel output transistors.

7- 8. (Cancelled)

9. (Currently amended) An integrated circuit comprising:

an IO PAD;

an output circuit coupled to at least said IO PAD; and

a stress circuit comprising at least one p-channel transistor, said stress circuit coupled to at least said output circuit and said IO PAD and adapted to limit a duration of

a high voltage across said output circuit when said output circuit is enabled, thereby reducing stress on said output circuit.

~~10-11. (Cancelled)~~

10-11. (Cancelled)

12. (Previously presented) The integrated circuit of Claim 9, wherein said at least one p-channel transistor comprises two stacked p-channel transistors.

13. (Currently Amended) The integrated circuit of Claim 9, wherein said output circuit comprises at least one output transistor.

14. (Currently Amended) The integrated circuit of Claim 13, wherein said at least one output transistor comprises an n-channel transistor.

15. (Currently Amended) The integrated circuit of Claim 13, wherein said at least one output transistor comprises two stacked n-channel transistors.

16. (Currently Amended) A method of controlling hot carrier injection stress comprising limiting a duration of a high voltage across an output device using a stress circuit comprising ~~at least one~~ two p-channel transistor ~~transistors~~ to limit said duration of said high voltage across said output device when said output device is enabled.

17. (Cancelled)

18. (Previously Presented) A method of reducing stress across an output circuit, comprising:

determining if the output circuit is tri-stated;

determining if a PAD voltage is greater than a predetermined voltage level;

enabling the output circuit;

turning on a stress circuit comprising at least one p-channel transistor, dissipating a voltage across the output circuit; and

preventing the output circuit from experiencing HCI stress.

19-21. (Cancelled)

22. (New) The method of Claim 18, wherein said at least one p-channel transistor is coupled to the output circuit.

23. (New) The method of Claim 18, wherein said stress circuit comprises two stacked p-channel transistors coupled to the output circuit.

24. (New) The method of Claim 18, wherein the output circuit comprises at least one n-channel output transistor.

25. (New) The method of Claim 18, wherein the output circuit comprises two stacked n-channel output transistors.

26. (New) An HCI stress circuit coupled to both an output circuit and an IO pad, the HCI stress circuit consisting of two stacked p-channel transistor devices, said two stacked p-channel transistor devices adapted to limit a duration of a high voltage across the output circuit thereby reducing hot carrier injection stress across the output circuit.

27. (New) The HCI stress circuit of Claim 26, wherein at least one of said two stacked p-channel transistor devices is coupled to the output circuit.

28. (New) The HCI stress circuit of Claim 26, wherein the output device comprises at least one n-channel output transistor circuit.

29. (New) The HCI stress circuit of Claim 26, wherein the output device comprises two stacked n-channel output transistor circuit.